



MS-7693

CPU

Ver:1.0

AMD M3 Phenom/Athlon 64 FX AM3/AM3R2

System Chipset

AMD RX980

ATI SB950

On Board Chip

FINTEK Super I/O -- F71889AD

LAN -- RTL8111EL

HD Codec --ALC892

ASM1042 USB3.0

BIOS -- SPI ROM 32M

Main Memory

DDR III X 4 (Max 8GB)

Expansion Slots

PCI-E X 16*1

PCI-E X 4 *1

PCI-E X 1 *2

PCI 2.2 Slot X 2

PWM

Controller--IUPI1601 4+1 Phase

Vcore 4 Phase (MOS HIGHX2 LOWX2)

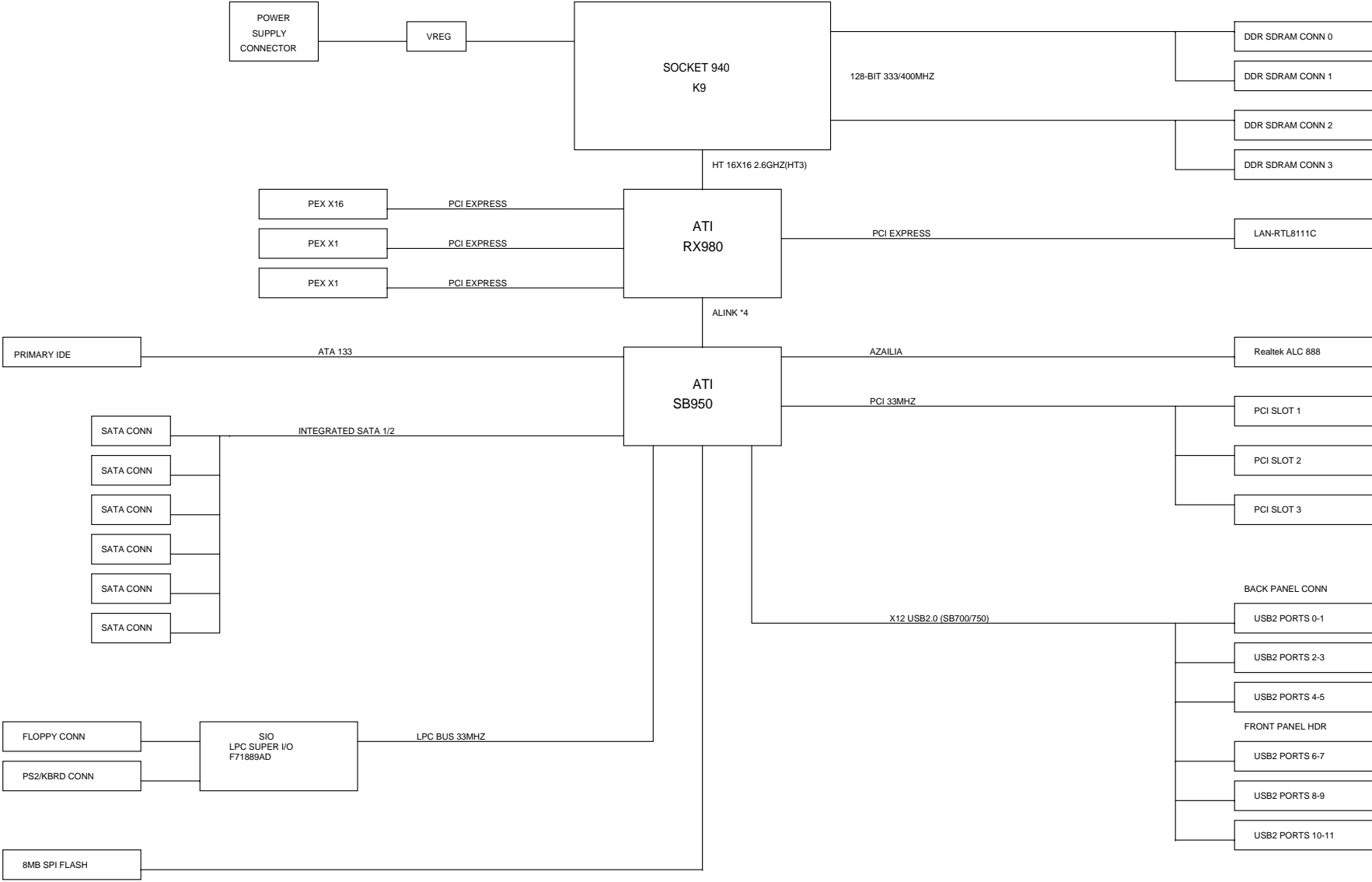
Vnb 1 Phase (MOS HIGHX1 LOWX2)

Clock Generator

Controller--RTM880N-793

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BLOCK DIAGRAM



Micro Star Restricted Secret		
Title	Block Diagram	Rev 1.0
Document Number	MS-7693	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, May 03, 2011 Sheet 2 of 32

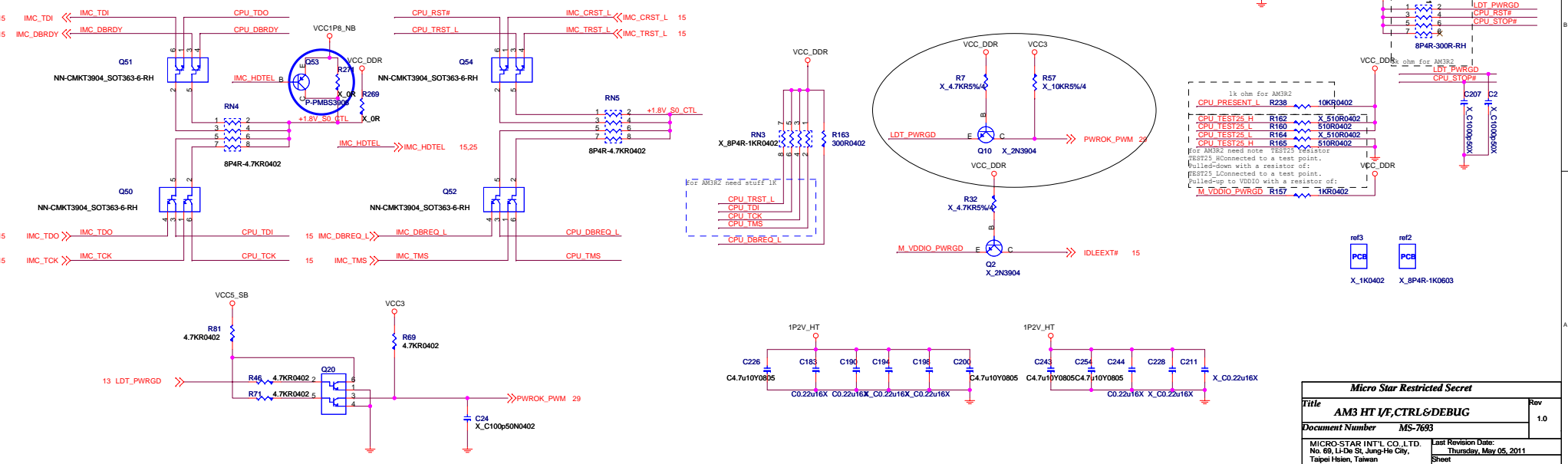
8 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
8 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
8 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
8 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]

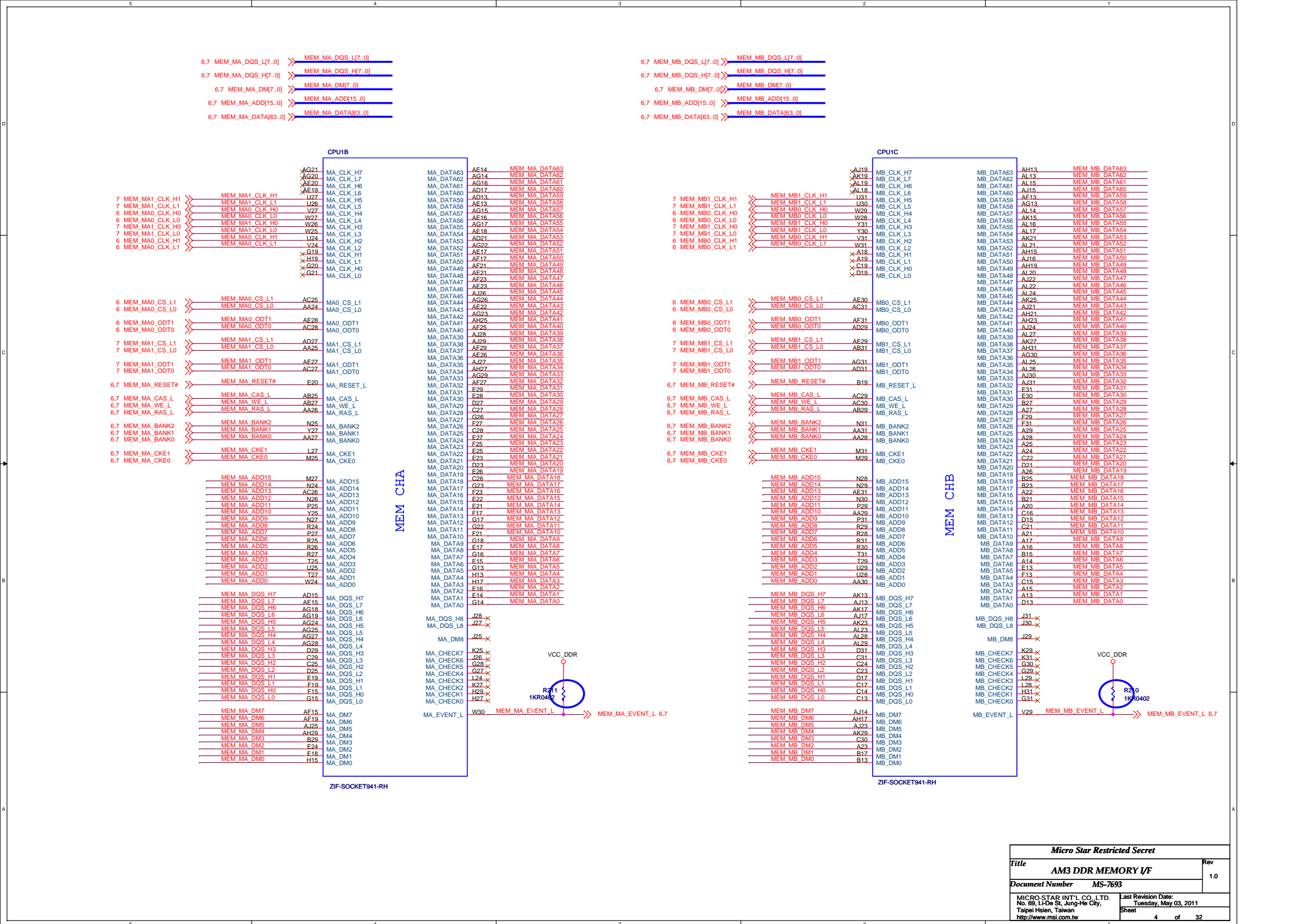
CPUA1A
8 HT_CLKIN_H1 >> N6
8 HT_CLKIN_L1 >> P6
8 HT_CLKIN_H0 >> N3
8 HT_CLKIN_L0 >> P3
8 HT_CTLIN_H1 >> V4
8 HT_CTLIN_L1 >> V5
8 HT_CTLIN_H0 >> U1
8 HT_CTLIN_L0 >> U1
8 HT_CADIN_H15 >> U6
8 HT_CADIN_L15 >> V6
8 HT_CADIN_H14 >> T4
8 HT_CADIN_L14 >> T5
8 HT_CADIN_H13 >> R6
8 HT_CADIN_L13 >> T6
8 HT_CADIN_H12 >> P4
8 HT_CADIN_L12 >> P5
8 HT_CADIN_H11 >> M4
8 HT_CADIN_L11 >> M5
8 HT_CADIN_H10 >> L6
8 HT_CADIN_L10 >> M6
8 HT_CADIN_H9 >> K4
8 HT_CADIN_L9 >> K5
8 HT_CADIN_H8 >> J6
8 HT_CADIN_L8 >> K6
8 HT_CADIN_H7 >> U3
8 HT_CADIN_L7 >> V3
8 HT_CADIN_H6 >> R1
8 HT_CADIN_L6 >> T1
8 HT_CADIN_H5 >> R3
8 HT_CADIN_L5 >> T3
8 HT_CADIN_H4 >> N1
8 HT_CADIN_L4 >> P1
8 HT_CADIN_H3 >> L1
8 HT_CADIN_L3 >> M1
8 HT_CADIN_H2 >> L2
8 HT_CADIN_L2 >> M2
8 HT_CADIN_H1 >> J1
8 HT_CADIN_L1 >> K1
8 HT_CADIN_H0 >> J2
8 HT_CADIN_L0 >> K2

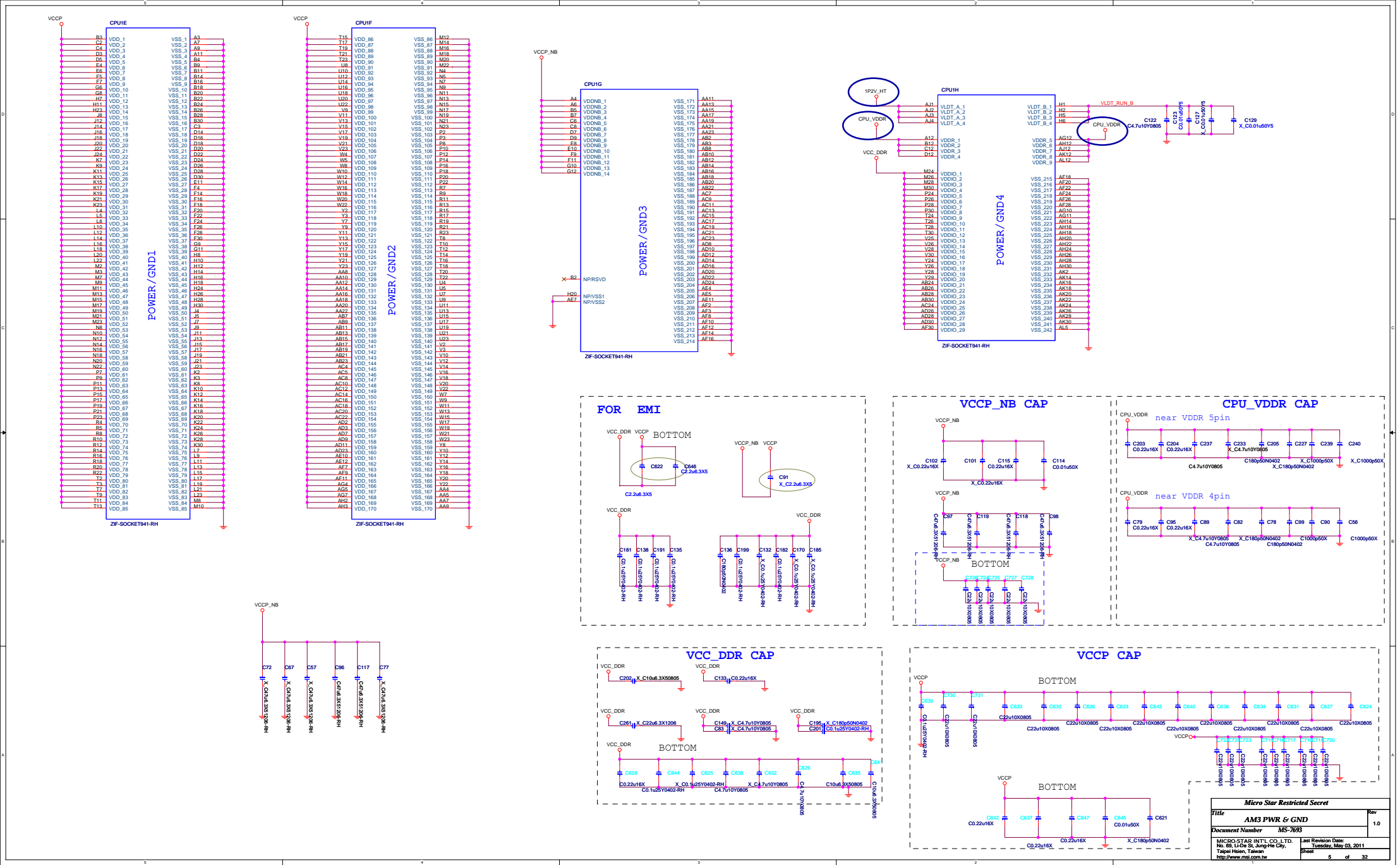
HT LINK

ZIF-SOCKET941-RH

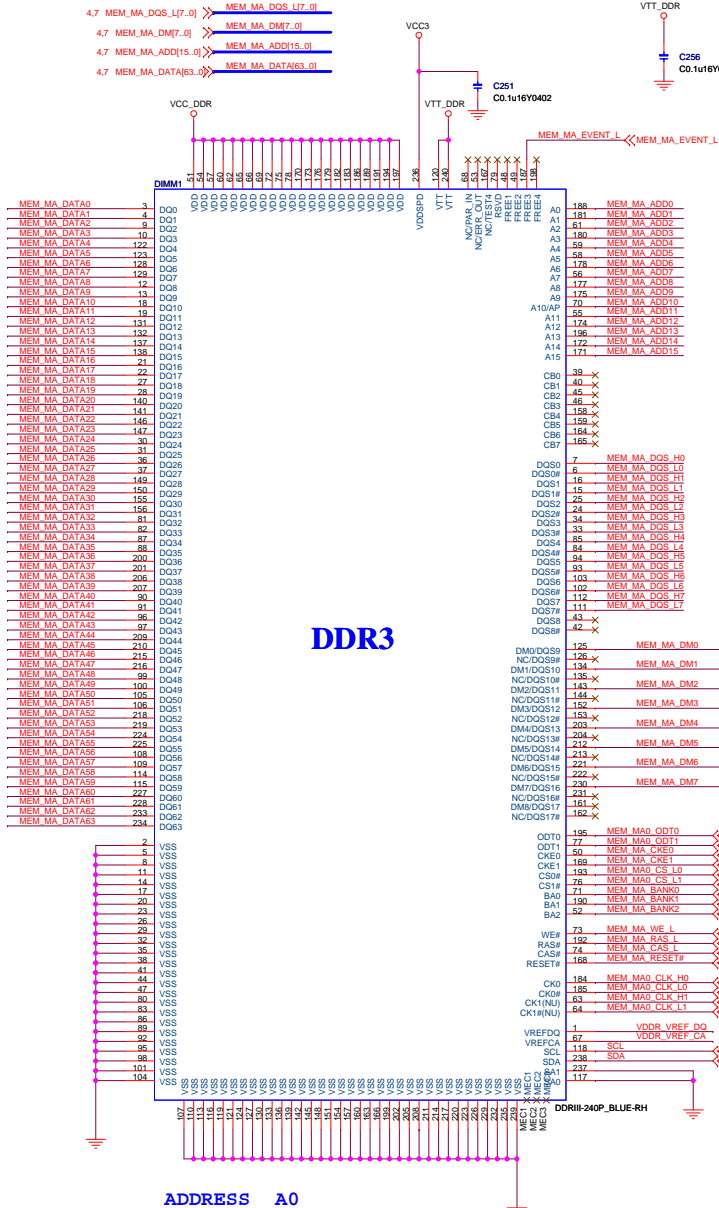
CPU output pin:TDO,DBRDY ; OTHERS :INPUT







4.7 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
 4.7 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
 4.7 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
 4.7 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
 4.7 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

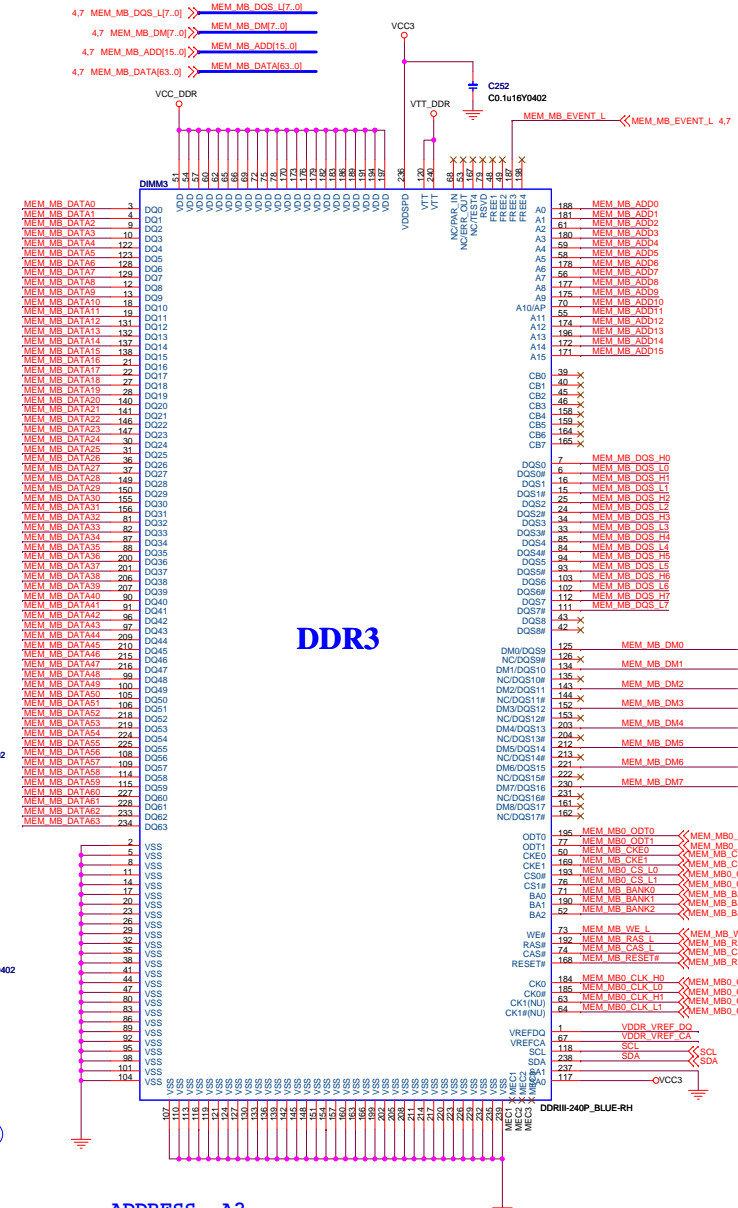


DDR3

SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6

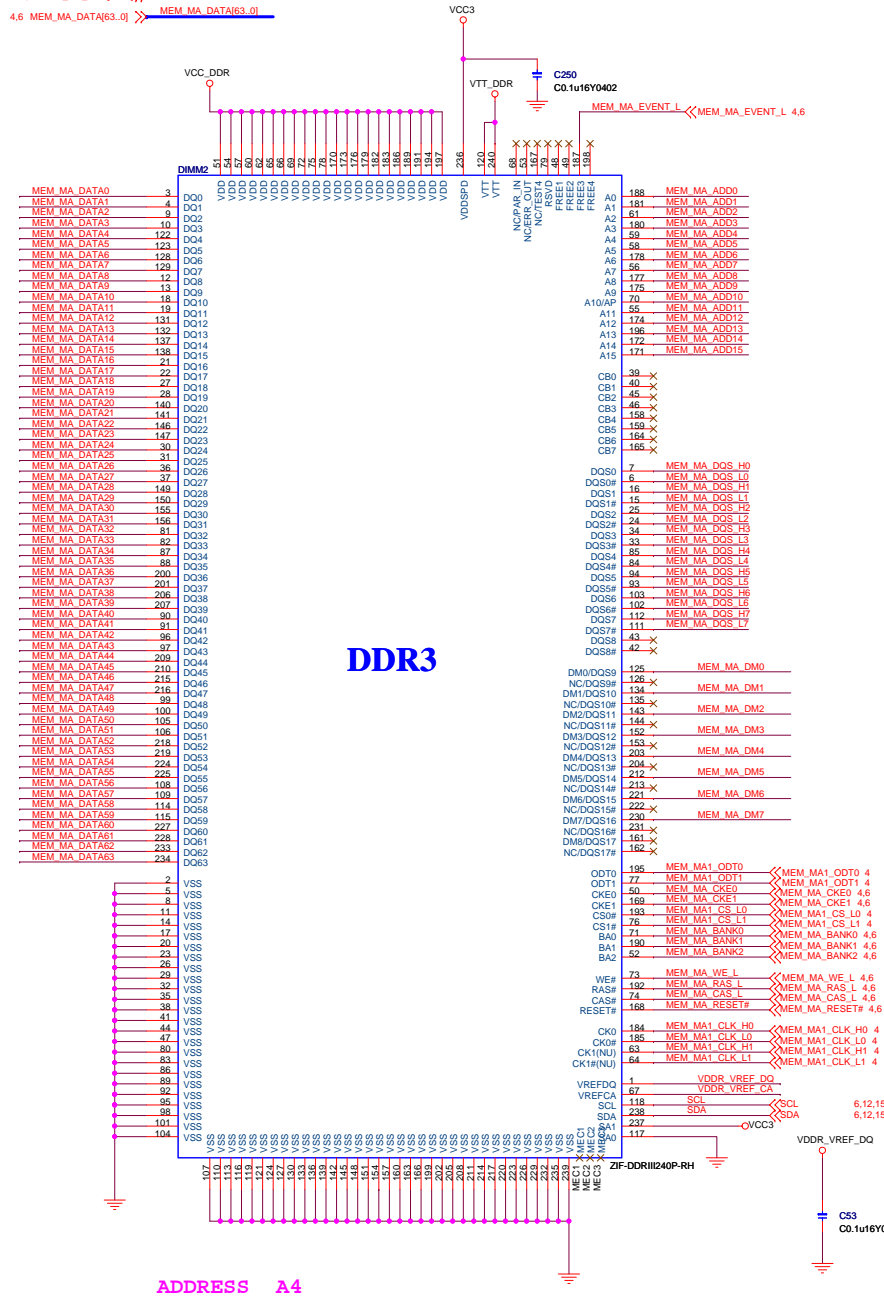
4.7 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
 4.7 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
 4.7 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
 4.7 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
 4.7 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]



DDR3

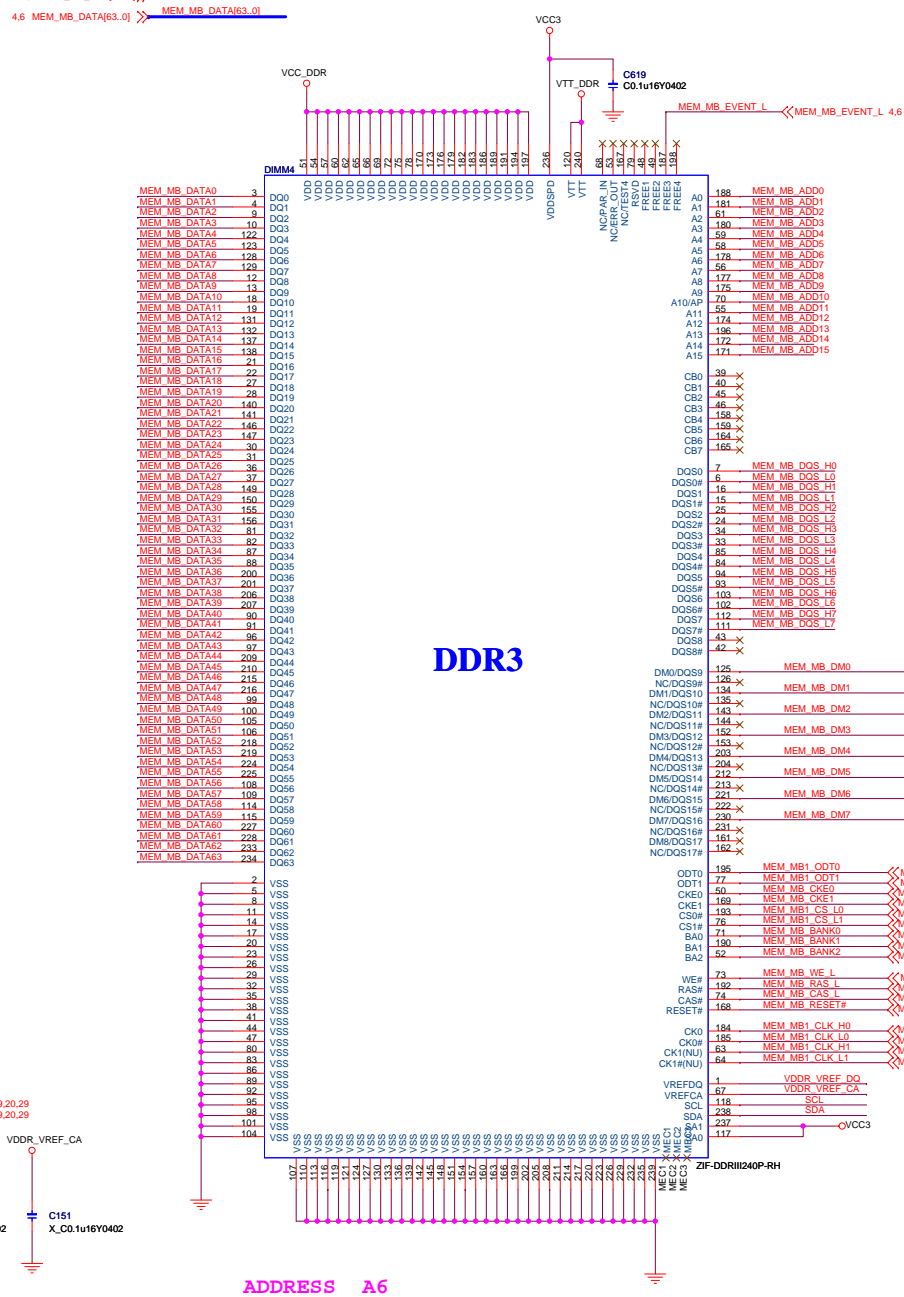
ADDRESS A2

4.6 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
4.6 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
4.6 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
4.6 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
4.6 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]



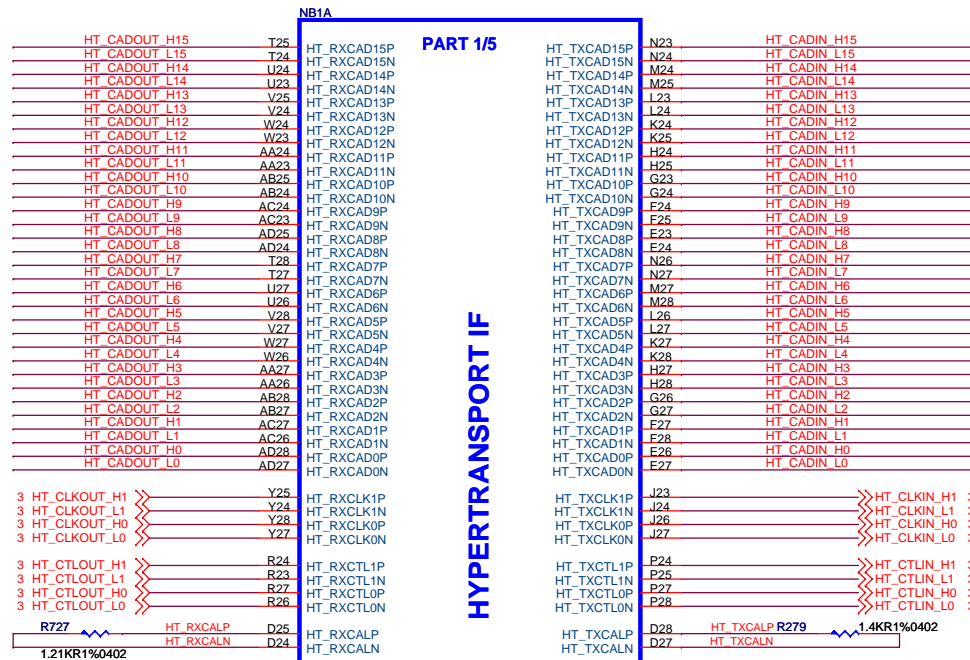
ADDRESS A4

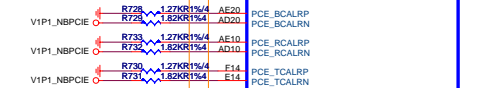
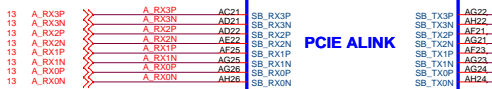
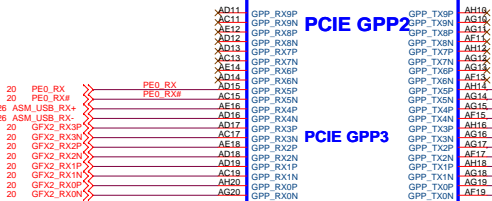
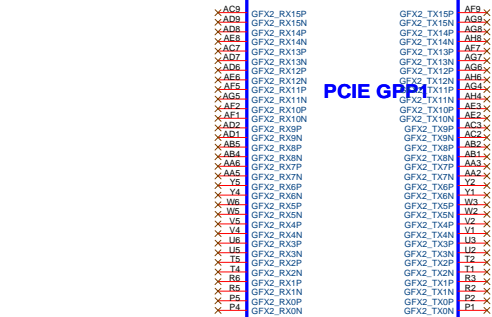
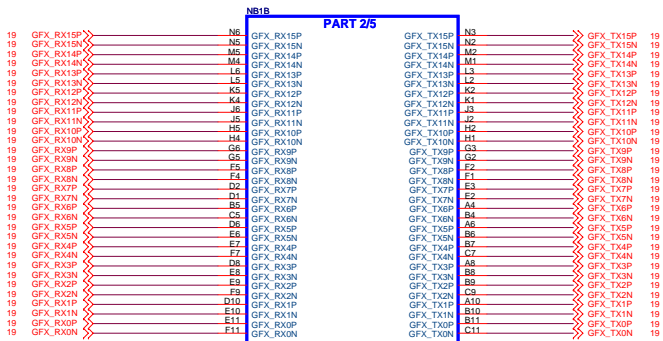
4.6 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
4.6 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
4.6 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
4.6 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
4.6 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]



ADDRESS A6

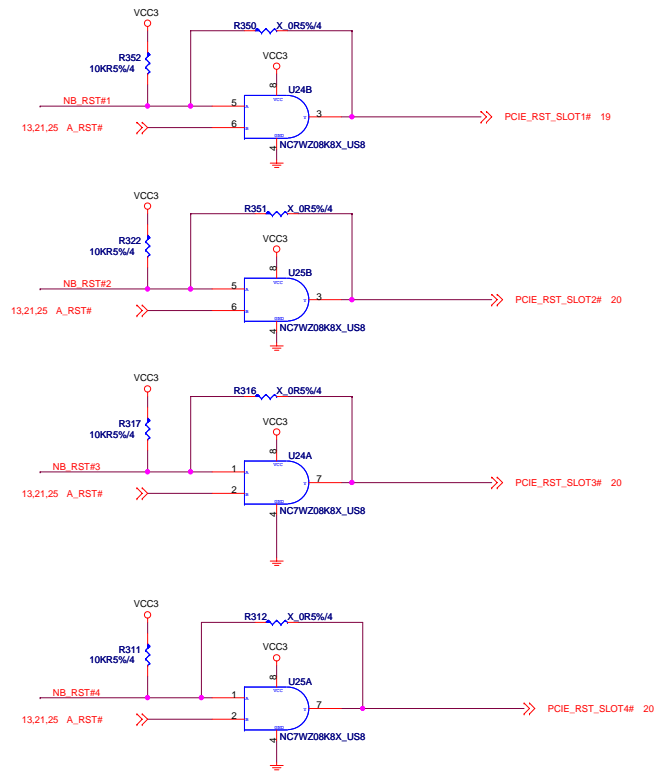
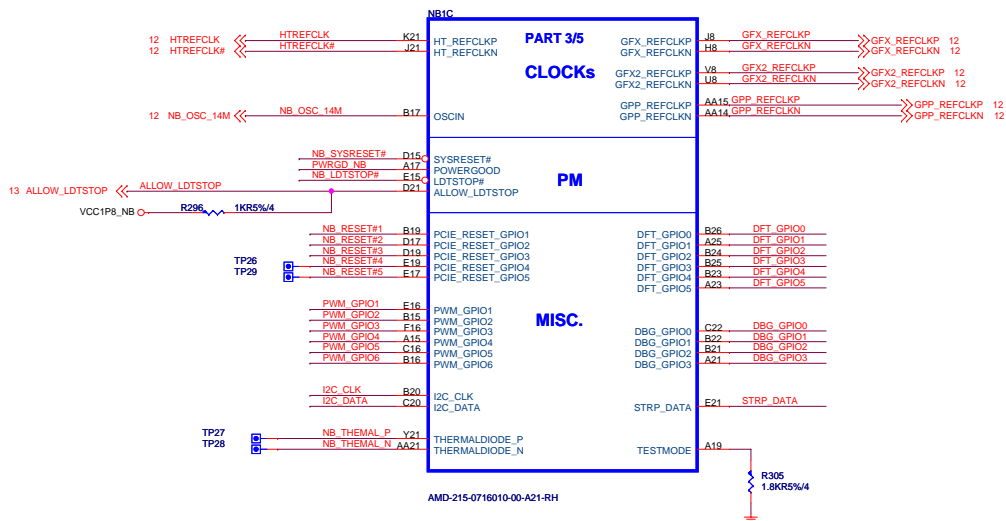
3 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
3 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
3 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
3 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]





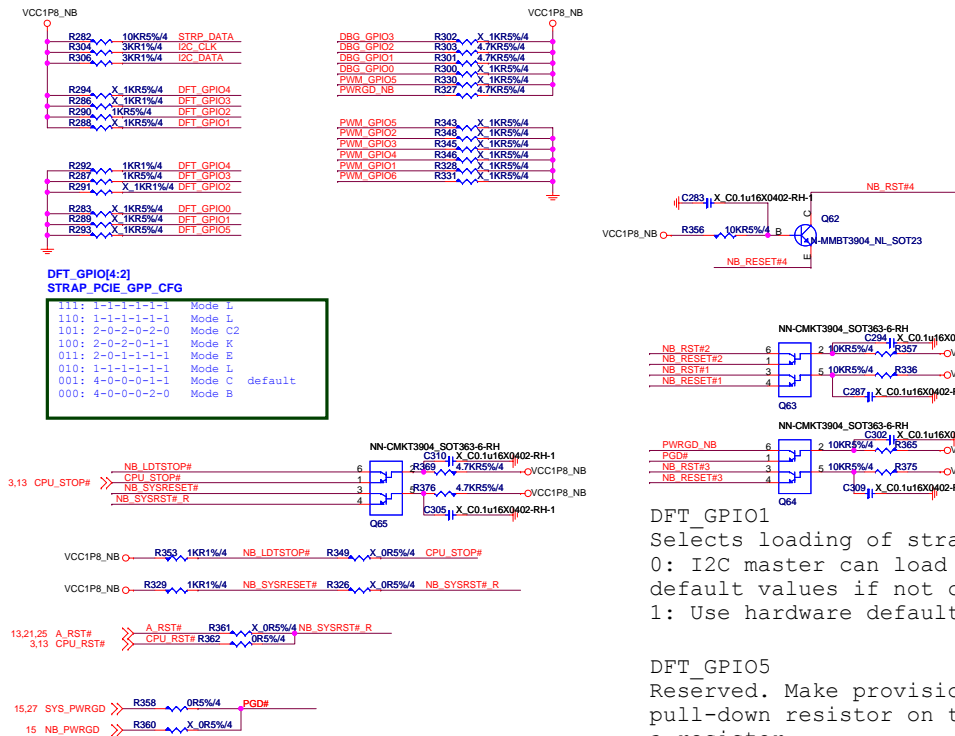
Spacing : 6mil

AMD-215-0716010-00-A21-RH



PWM_GPIO[5:2]
Reserved.
Make provision for an external pull-down resistor on each of the pins, but do not install a resistor.

DFT_GPIO0
Reserved. Make provision for an external pull-down resistor on this pin, but do not install a resistor.



PART 5/5

GROUND

NB1E
AMD-215-0716010-00-A21-RH

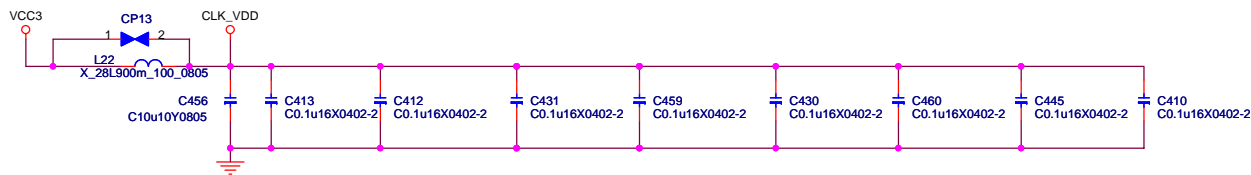
normal 13.6W

PART 4/5

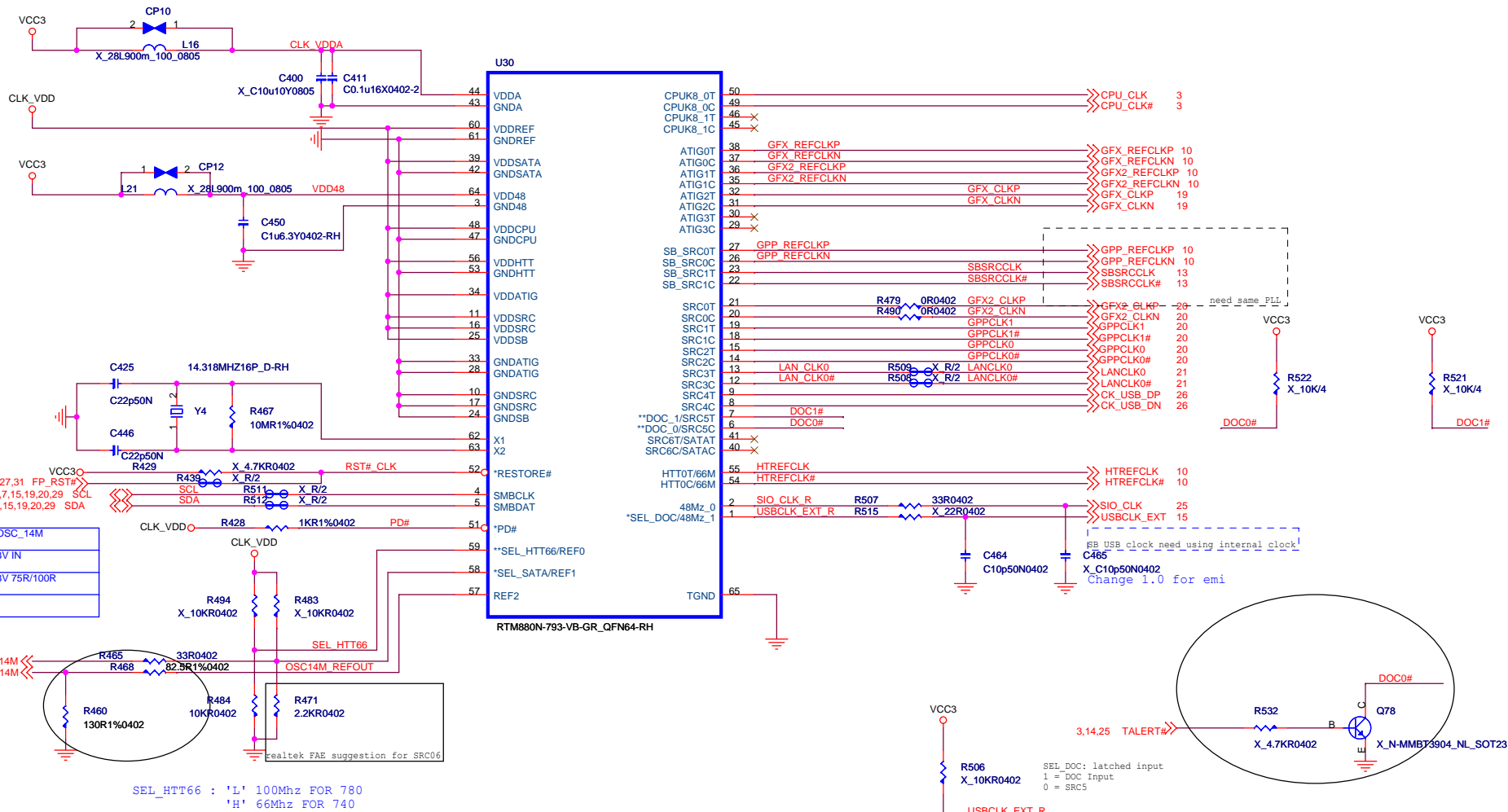
POWER

AMD-215-0716010-00-A21-RH

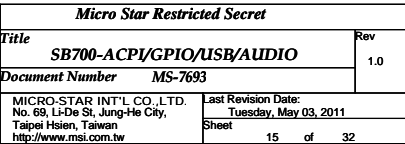
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Title	RX890-POWER	Rev
Document Number	MS-7693	1.0
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St., Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, May 06, 2011
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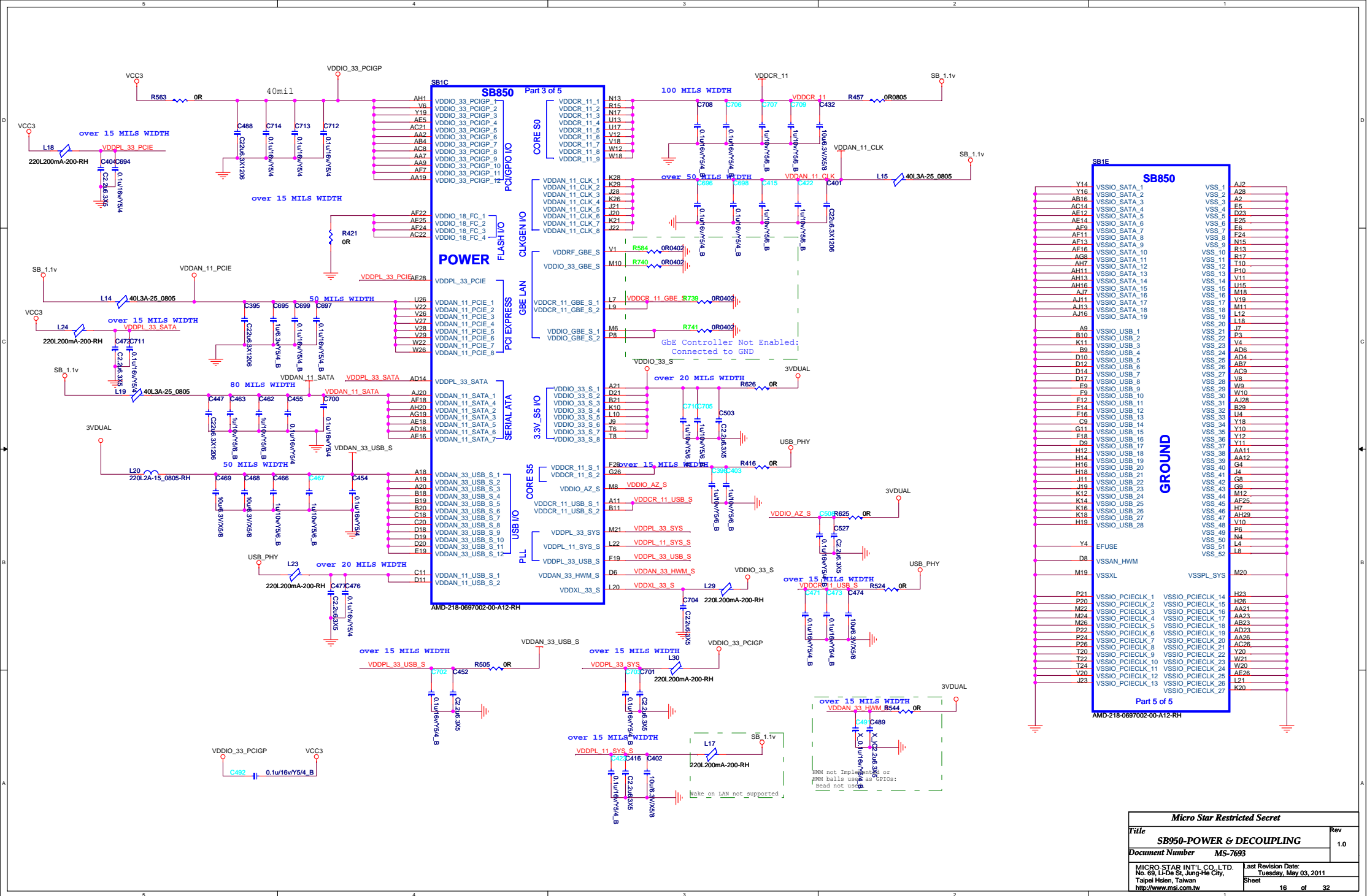


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U19 AS POSSIBLE
- 2- ROUTE ALL CPUCCLK/#, NBSRCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U19 POWER PIN



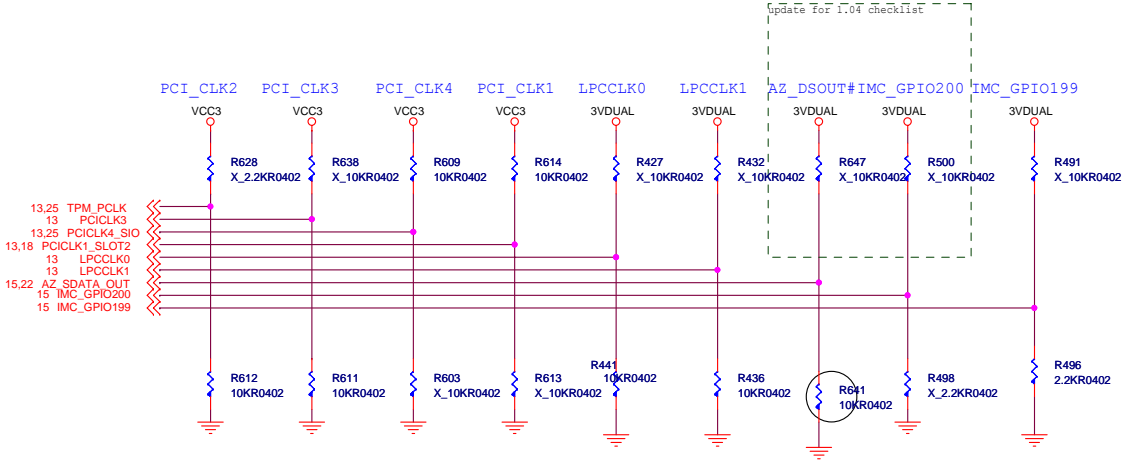
Micro Star Restricted Secret		
Title Clock Generator RTM880N-793		Rev 1.0
Document Number MS-7693		
MICRO-STAR INT'L CO. LTD. No. 69, Li-De St., Jung-Hsi City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, May 03, 2011 Sheet 12 of 32





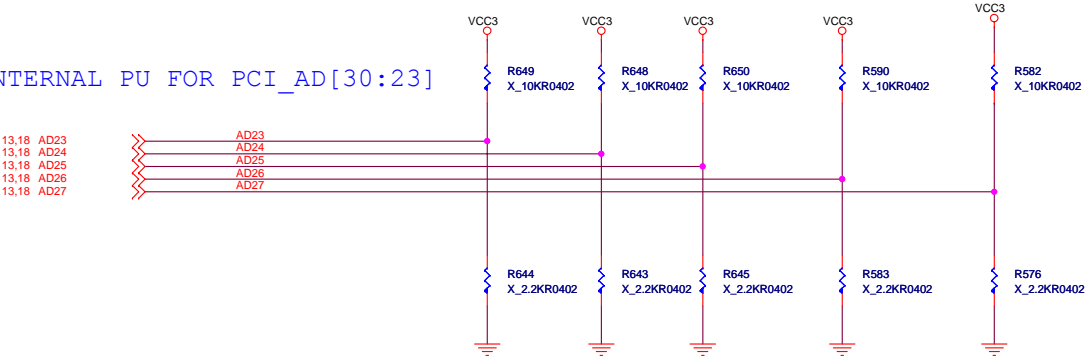
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_DOUT#	IMC_GPIO200	IMC_GPIO199
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE DEFAULT	UEC ENABLE	CLKGEN ENABLED		ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	FORCE PCIE GEN1	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE	DISABLE EC DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	L, H = LPC ROM L, L = FWH ROM	

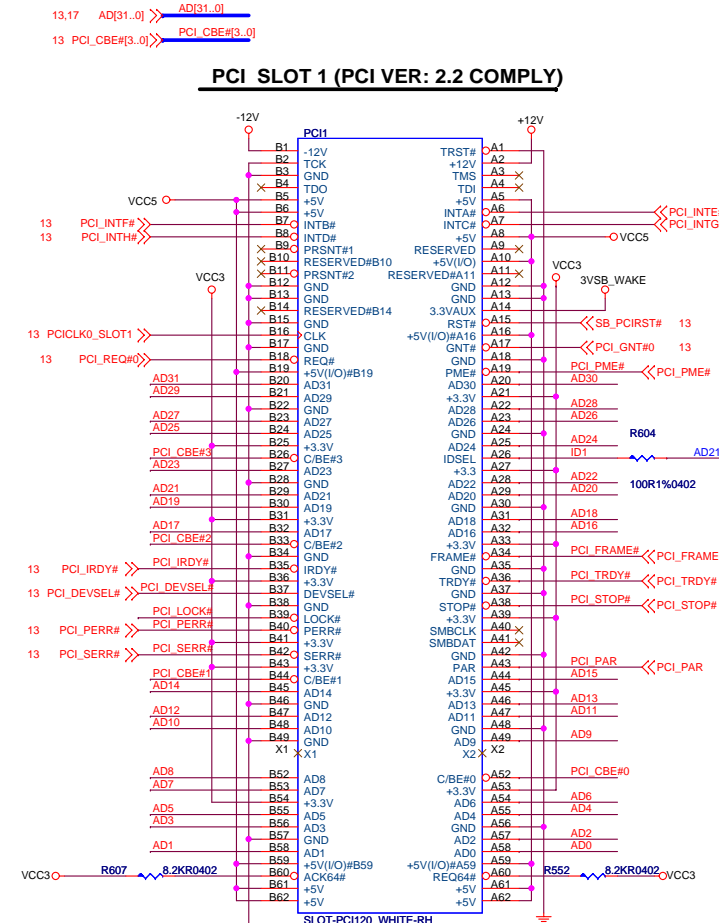
SB800 HAS 15K INTERNAL PU FOR PCI_AD[30:23]



DEBUG STRAPS

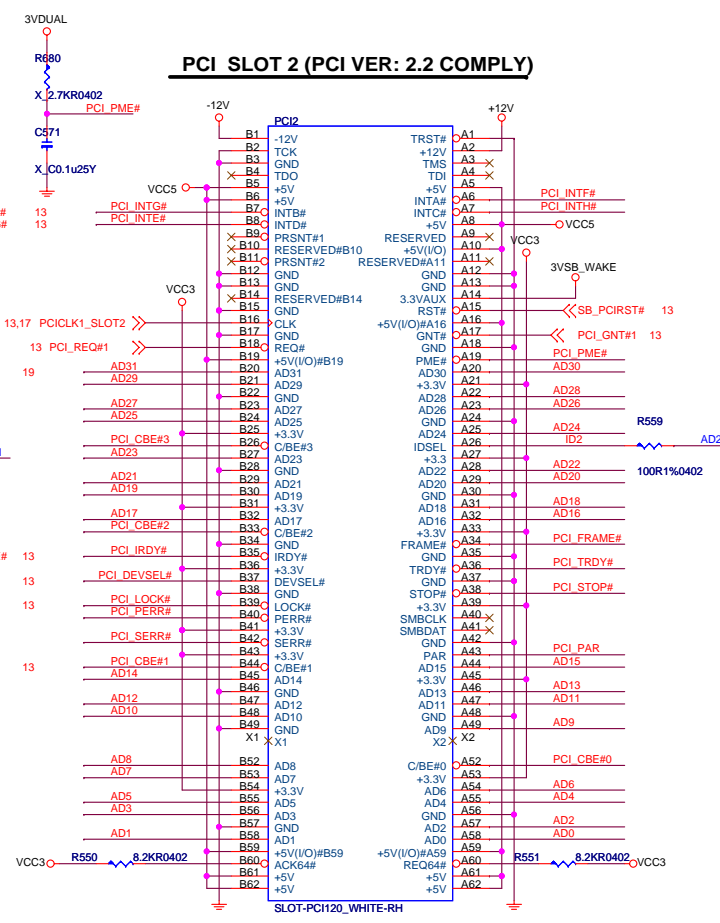
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



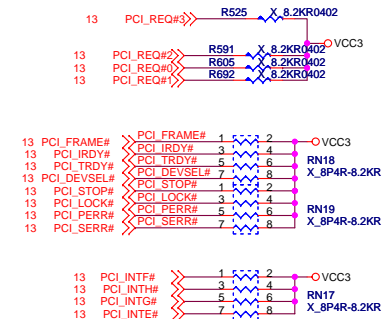
IDSEL = AD21
MASTER = PCI_REQ#0
PCI_GNT#0

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



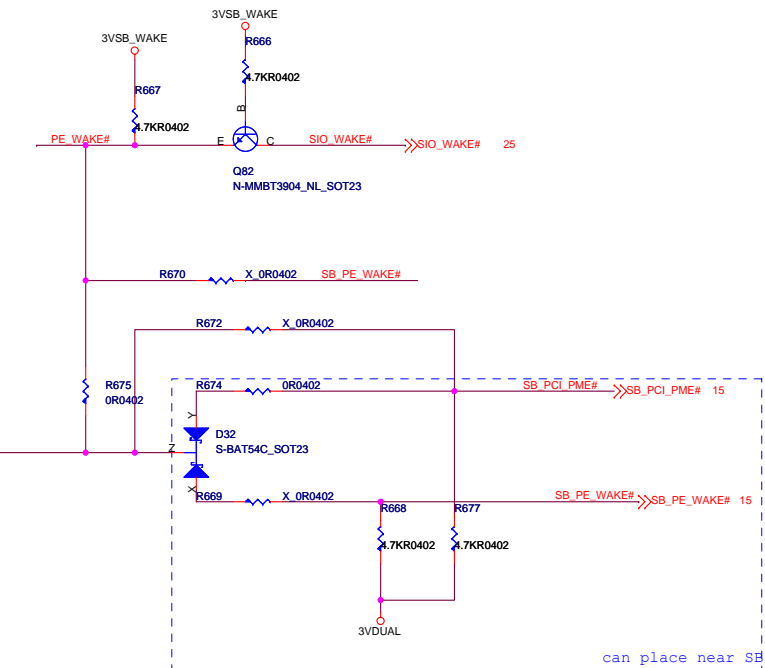
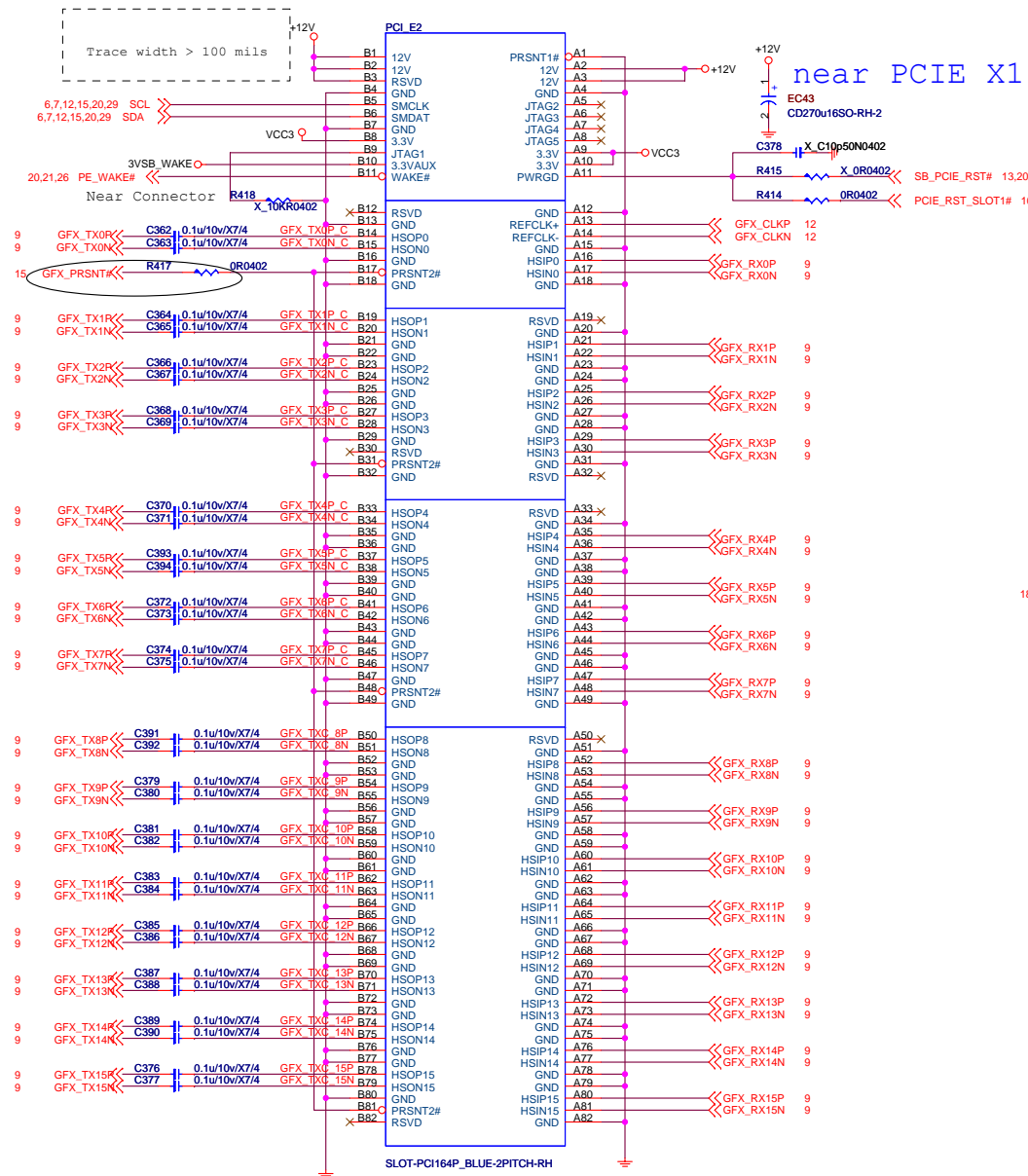
IDSEL = AD22
MASTER = PCI_REQ#1
PCI_GNT#1

PCI PULL-UP / DOWN RESISTORS



Micro Star Restricted Secret		
Title	PCI Slot 1,2,3& PCI Extender	Rev 1.0
Document Number	MS-7693	
MICRO-STAR INT'L CO., LTD.		Last Revision Date:
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Taipei Hsien, Taiwan		Sheet 18 of 32
http://www.msi.com.tw		

PCI EXPRESS 16



Digital Switch
SEL pin

SEL (X8 X8#)	Output	X8 SW	PCI-E Slot 1/2
Low	0a	Low	X8 / X8
Hi	0b	Hi	X16 / 0

PCI EXPRESS X4

near PCIE X3

EC51
CD270u16SO-RH-2

Trace width > 100 mils

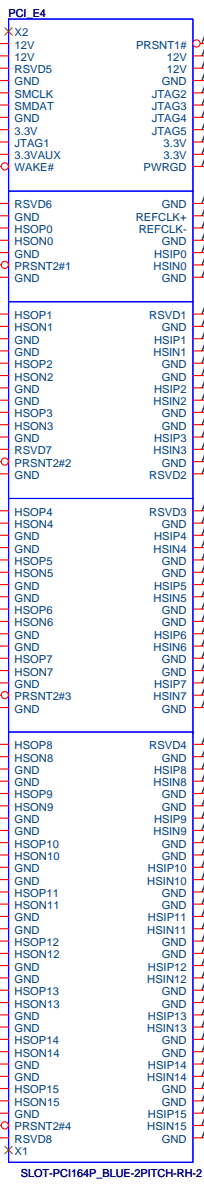
6,7,12,15,19,29 SCL
6,7,12,15,19,29 SDA
VCC3
3VSB_WAKE#
19,21,26 PE_WAKE#

9 GFX2_TX0P
9 GFX2_TX0N
15 GFX2_PRSTN#
9 GFX2_TX1P
9 GFX2_TX1N
9 GFX2_TX2P
9 GFX2_TX2N
9 GFX2_TX3P
9 GFX2_TX3N

PEX8_SLOT_PRSTN#

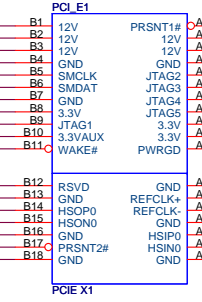
PEX8_SLOT_PRSTN#

PEX8_SLOT_PRSTN#

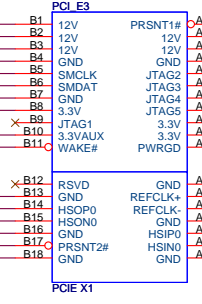


SLOT-PC164P_BLUE-2PITCH-RH-2

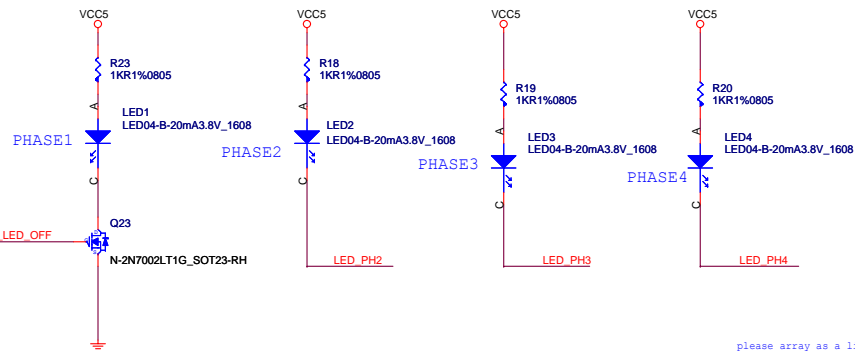
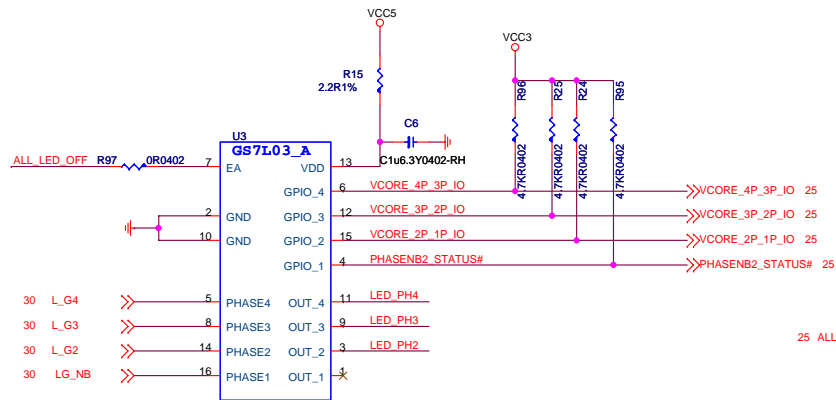
PCI-Express x1 SLOT 1



PCI-Express x1 SLOT 1



Micro Star Restricted Secret		
Title	PCIE X1 Slot 1, 2	Rev 1.0
Document Number	MS-7693	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, May 03, 2011 Sheet 20 of 32



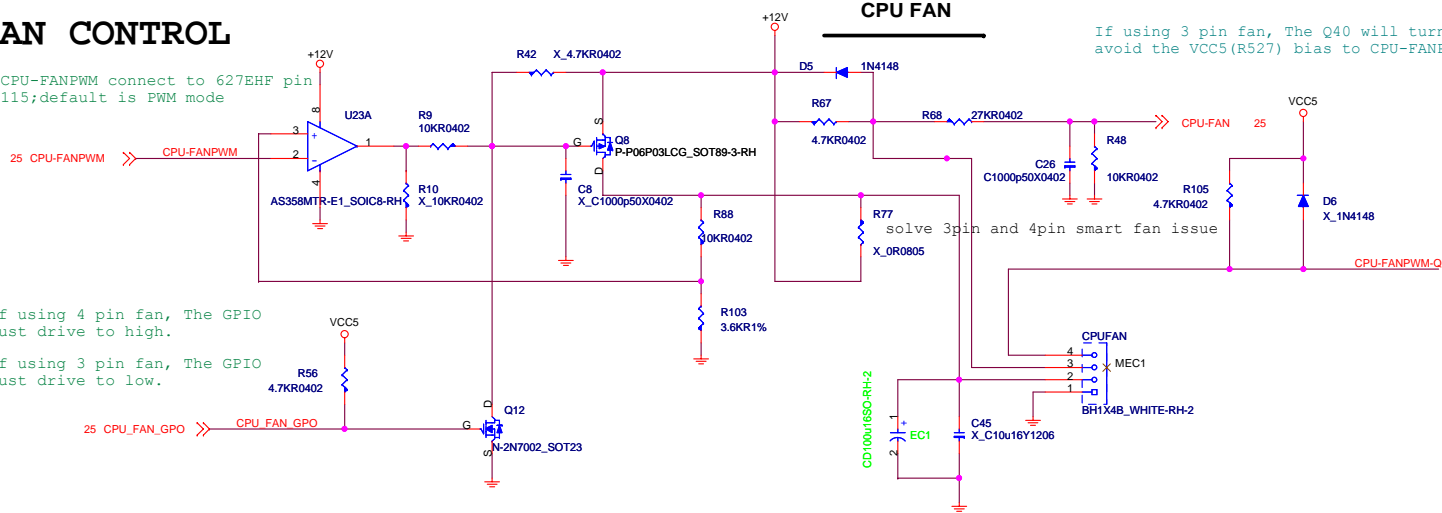
please array as a line

FAN CONTROL

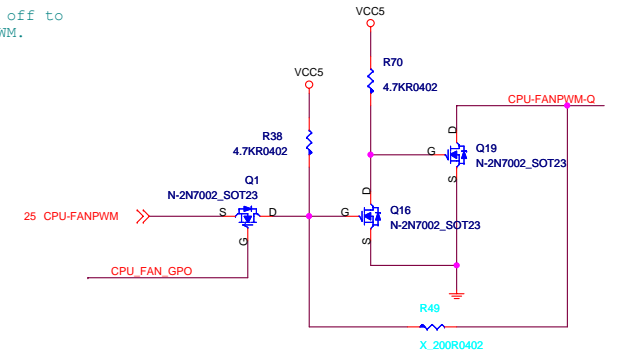
CPU-FANPWM connect to 627EHF pin 115; default is PWM mode

If using 4 pin fan, The GPIO must drive to high.

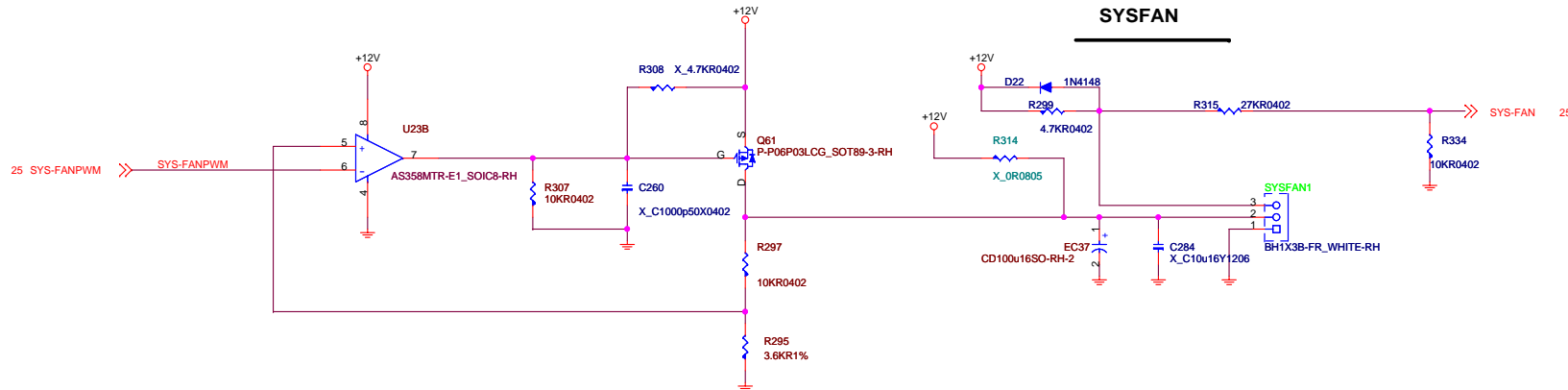
If using 3 pin fan, The GPIO must drive to low.



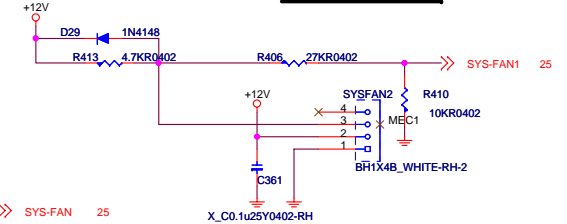
If using 3 pin fan, The Q40 will turn off to avoid the VCC5(R527) bias to CPU-FANPWM.



SYSFAN



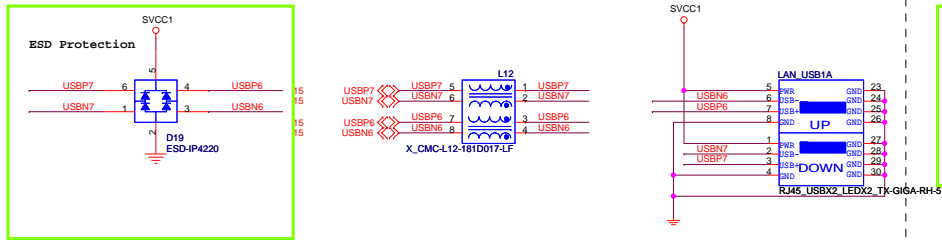
SYS FAN2



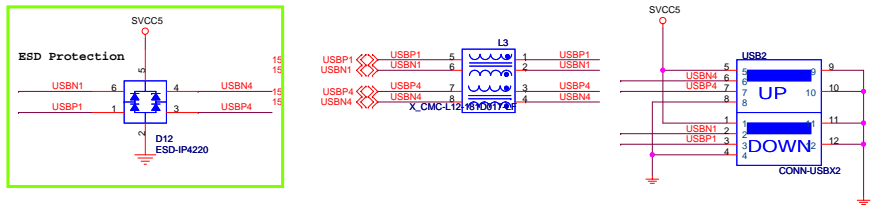
Micro Star Restricted Secret

Title		Rev
IDE Conn/FAN/LPT/SATA		1.0
Document Number		MS-7693
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipet Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, May 03, 2011
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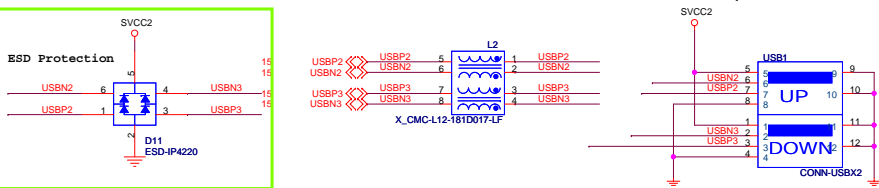
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



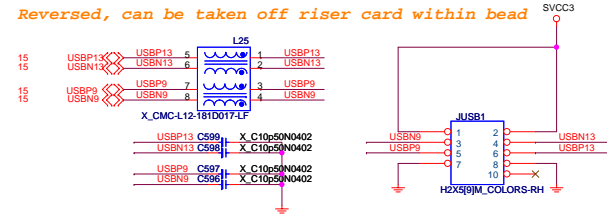
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



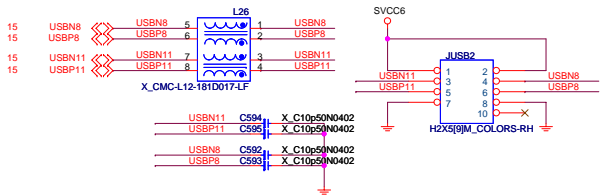
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



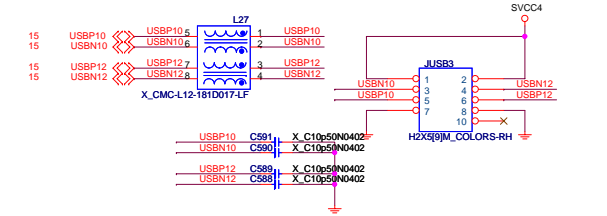
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



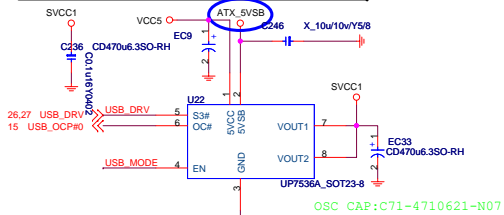
FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



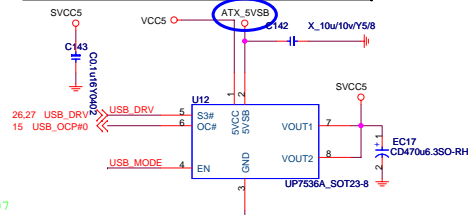
FRONT PANEL USB CONNECTOR FOR USB PORT 10,11



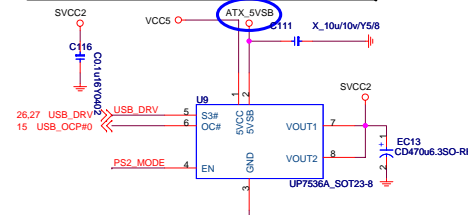
POWER CIRCUIT FOR USB PORT 0,1



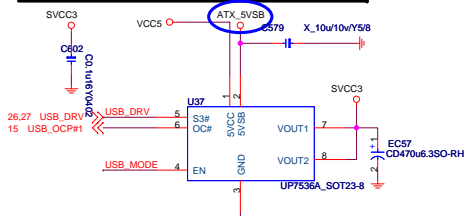
POWER CIRCUIT FOR USB PORT 2,3



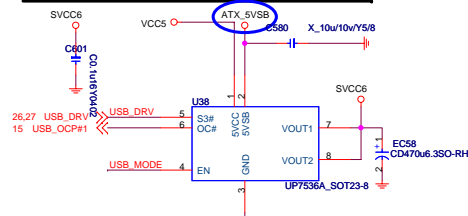
POWER CIRCUIT FOR USB PORT 4,5



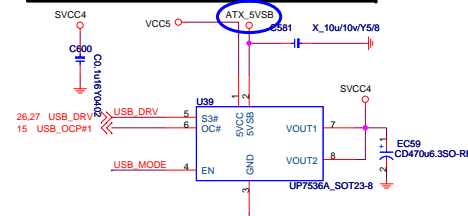
POWER CIRCUIT FOR USB PORT 6,7



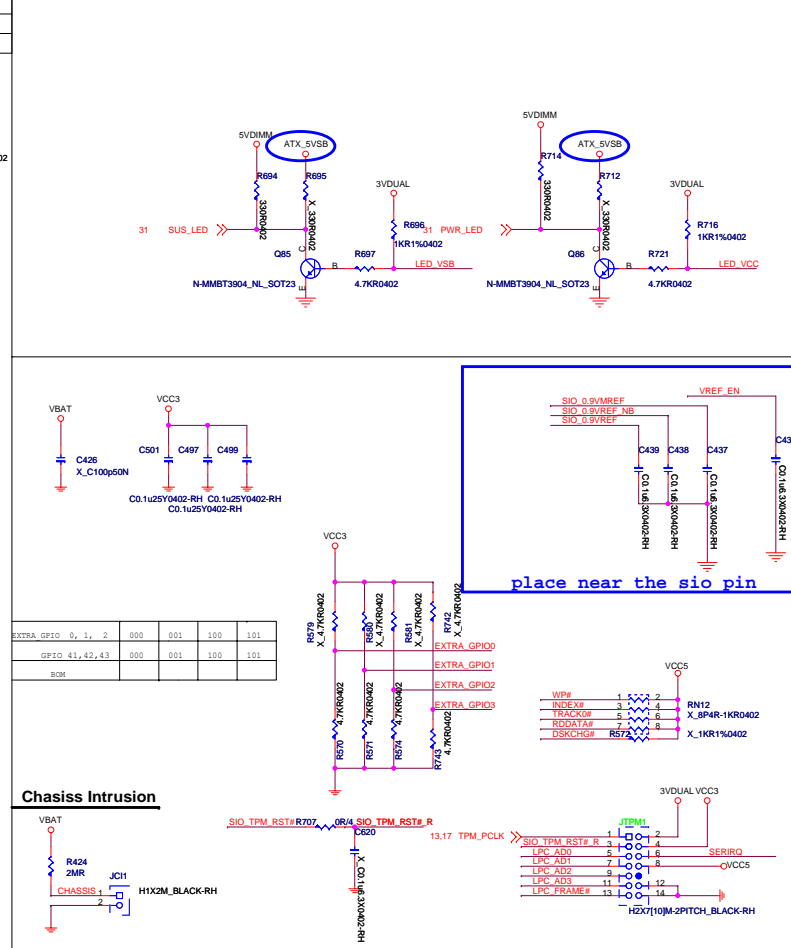
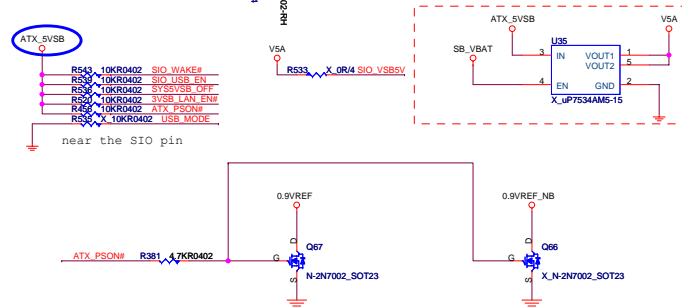
POWER CIRCUIT FOR USB PORT 8,9



POWER CIRCUIT FOR USB PORT 10,11



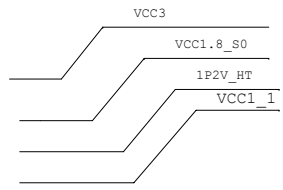
LPC SUPER I/O F71889

[illegible]

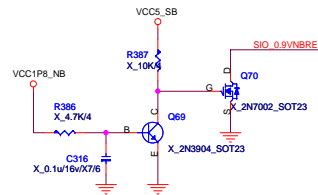
NOTE: LOCATE CLOSE 5_VRM mosfet_for VRM mosfet temperature detect only

Micro Star Restricted Secret		
Title	ACPI BY UPI	Rev
Document Number	MS-7693	1.0
MICRO-STAR INT'L CO., LTD. No. 69, U-De St., Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, May 03, 2011 Sheet 27 of 32

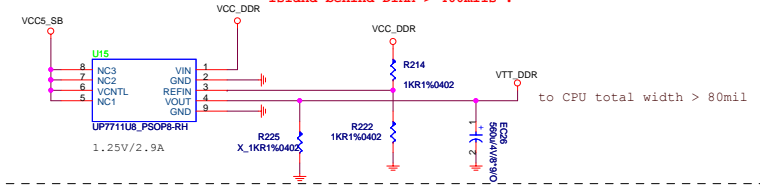
RX780 power up sequence



Reserve for RX980 POS

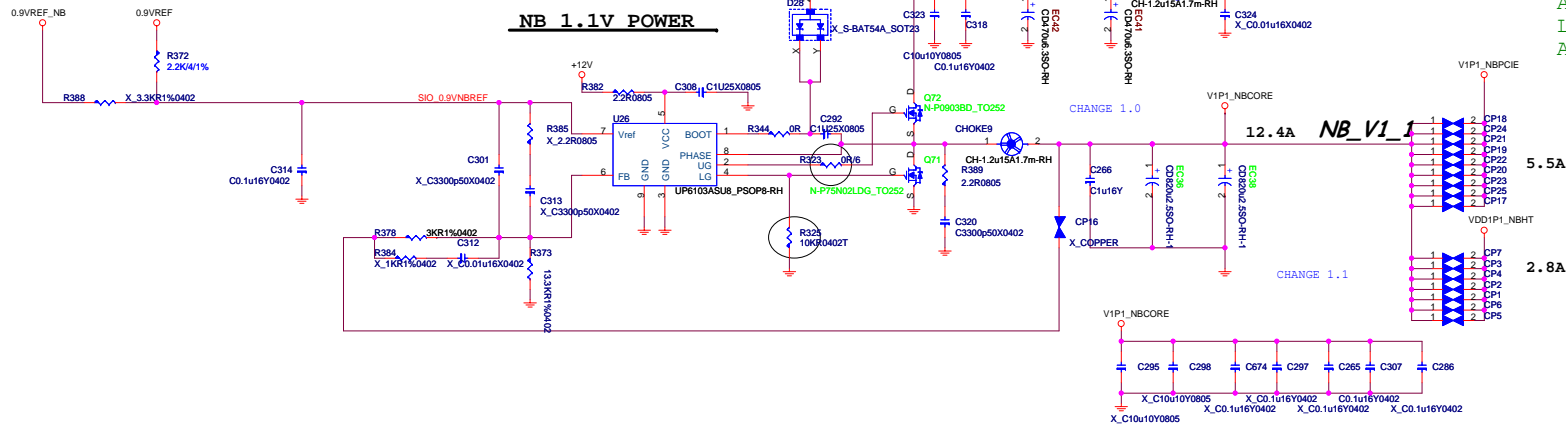


DDR VTT Power



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

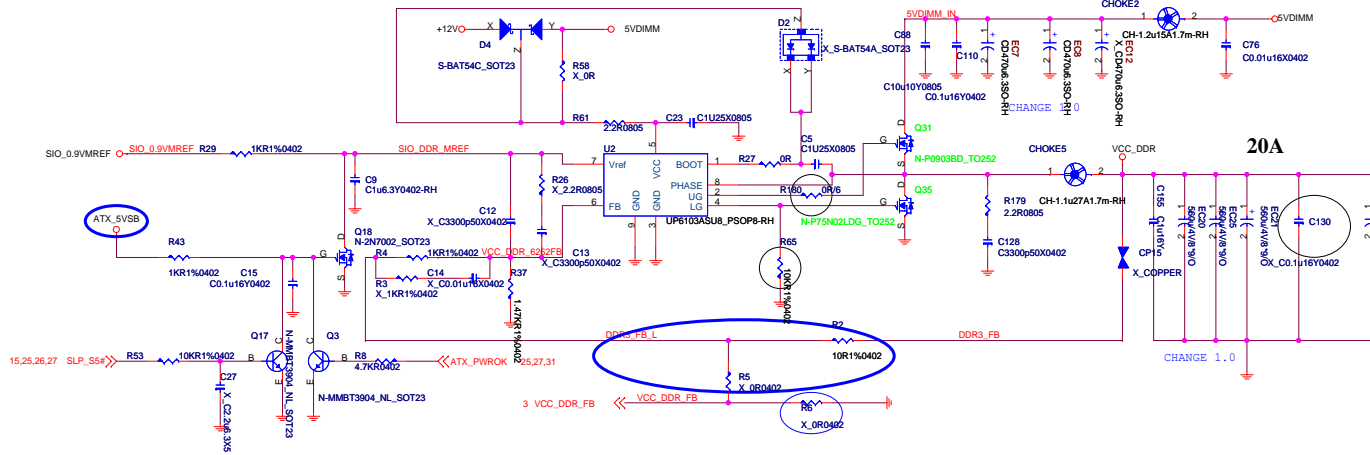
NB 1.1V POWER



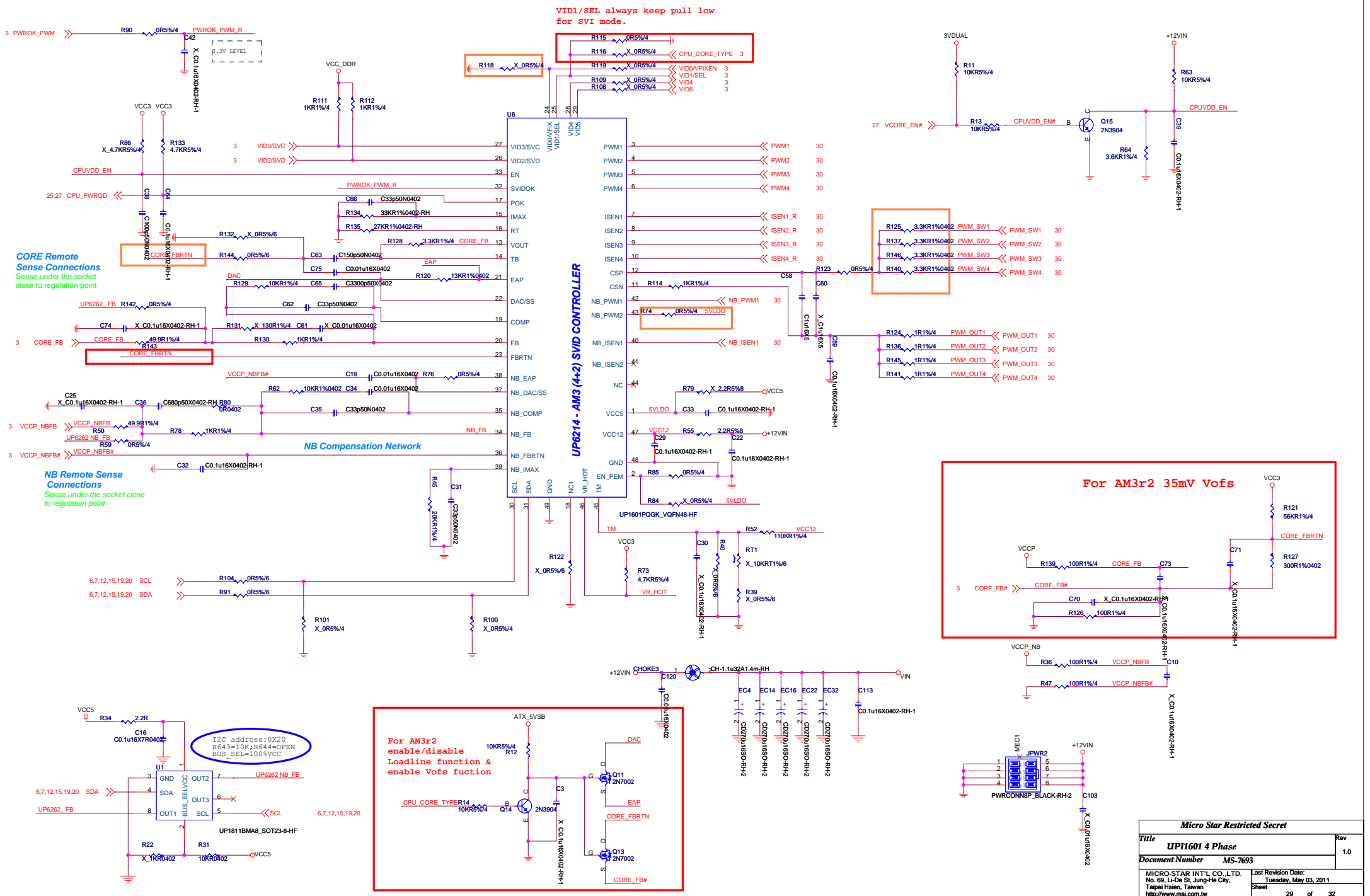
H-MOS: D03-0903BDB-N03
AVL: D03-0480900-O05
L-MOS: D03-75N022B-N03
AVL: D03-0480600-O05

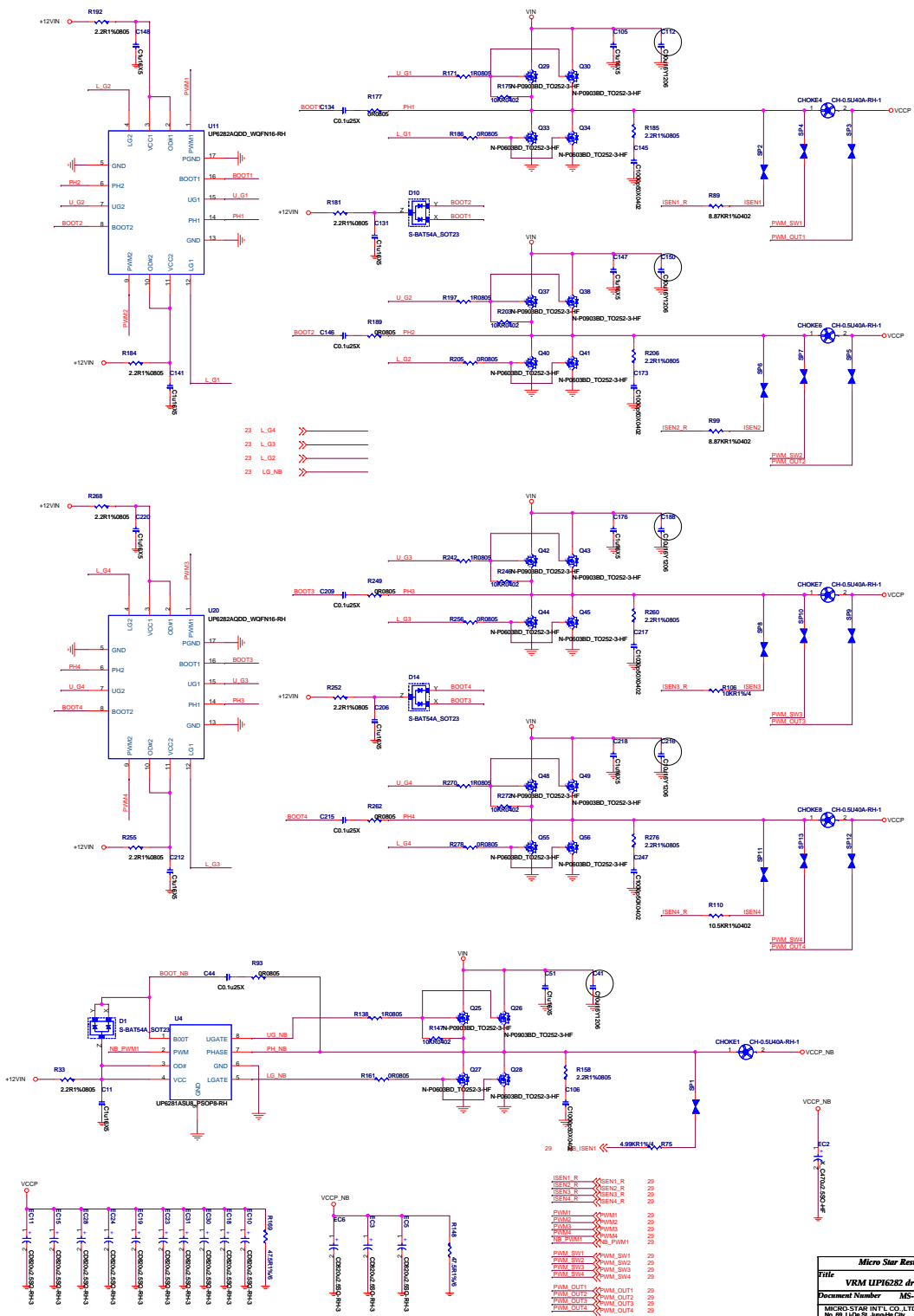
DDR III 1.5V POWER

VCC_DDR

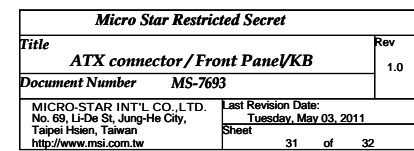


Micro Star Restricted Secret	
Title	VCC_DDR&VCC1_1
Document Number	MS-7693
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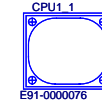
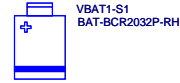
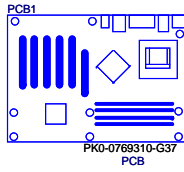
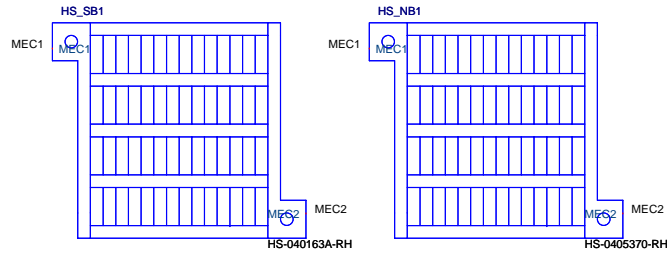




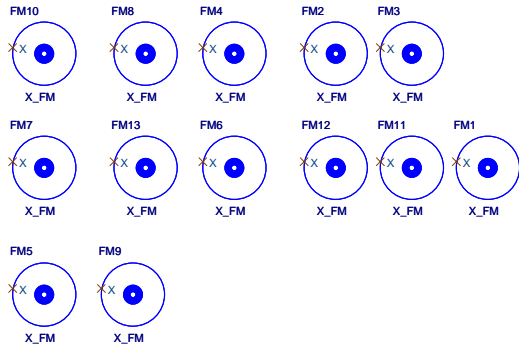
Intel Front Panel



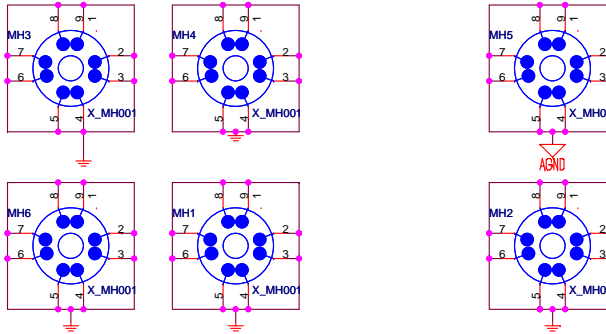
MK1
G51-M1SP990-Q13



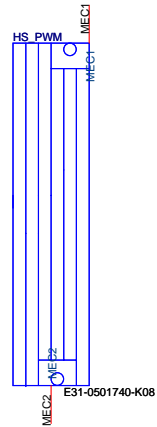
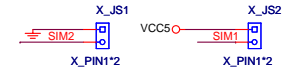
Optics Orientation Holes



Mounting Holes



Simulation



Micro Star Restricted Secret		
Title	MANUAL PARTS	Rev 1.0
Document Number	MS-7693	
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